

REMARKS

The present application includes pending claims 1-4, all of which remain rejected. Claims 1-4 remain rejected under 35 U.S.C. 103(a) as being unpatentable over GB 2134045 ("Slomianny") and United States Patent No. 4,567,570 ("Peer"). The Applicants respectfully traverse this rejection for at least the reasons previously discussed during prosecution and the following:

I. The Proposed Combination Does Not Teach Or Suggest All The Limitations Of Claims 1-4

Claim 1 of the present application recites, in part, the following:

Processing means to process the stored print data, wherein the processing means, in use,

* * *

(d) sequentially reads one or more print data sub-elements from the memory locations associated with one pre-determined time period;

* * *

characterized in that step (d) is repeated for a subsequent pre-determined time period for each pulse generated by the pulse generating means.

The Office Action acknowledges that Slomianny does not disclose the limitations noted above. *See* February 26, 2007 Office Action at page 3, and August 14, 2006 Office Action at page 3.

The Office Action asserts, however, that Peer makes up for this deficiency. In particular, the previous Office Action cited Peer at column 1, line 65 to column 2, line 13, column 5, lines 3-35, and column 6, lines 19-30 as disclosing the limitations that are not found in Slomianny. *See* August 14, 2006 Office Action at pages 3-4. The present

Office Action also cites Peer at lines 5-19, column 8, lines 35-40, and Figure 6. *See* February 26, 2007 Office Action at pages 4-5.

The Applicants now turn to these cited portions of Peer. Peer at column 1, line 65 to column 2, line 13 recites the following:

The present inventor recognized that the matrix printer systems available for driving a print head consisting of slanted or inclined print elements were very complex, requiring a high component count and complicated data handling. Accordingly, he designed the present inventive data converter system for driving a slanted print head of a matrix printer with a system having a low component count via the use of a microprocessor and a short processing time via unconventional microprocessor-memory-I/O (Input/Output) design and implementation.

Included in the present invention are input latch means for receiving individual vertical columns of imaging input data bits that is operable for dividing each column into byte column segments, equal in number to the number of banks of memory means.

This passage of Peer merely discloses that latch means receive vertical columns of imaging input data bits and divide each column into byte column segments, equal in number to the number of banks of memory means. There is nothing in this passage, however, that teaches or suggests “sequentially reading one or more print data sub-elements from the memory locations associated with one pre-determined time period” and **“repeating” the sequentially reading step “for a subsequent pre-determined time period for each pulse generated by the pulse generating means,”** as recited in claim 1 of the present application.

Next, Peer at column 5, lines 3-35 states the following:

In FIG. 4, a typical matrix printer system 37 is shown in a block diagram, and includes in this example a slant printer head 39. Also in this example, a data processor 41 is shown

as the host machine supplying columns of vertically oriented imaging data bits to the printer 37 for printing out a desired image on a print medium. The imaging data bits are supplied to printer 37 over a data bus 43, and control signal buses 45, 47, and 49 are used for passing control signals between the matrix printer 37 and the data processor 41. Also included in the matrix printer 37 are a vertical-to-slant data converter 51 for converting the received vertically oriented imaging data bits into control signals for operating the print element drivers 53 for controlling the slanted print head to print the imaging data upon the print medium in the same vertical orientation of the originally received imaging data bits, or in italics, if desired. Also, a motor controller 55, partially controlled by data processor 41, provides control signals for operating motor drivers 57 in controlling the operation of a carriage motor 59 for moving the print head 39, and a platen motor 61 for moving the print medium placed upon the platen of the printer to a desired position for initiating a new line of print. A position encoder 63 detects the column position of the print head 39 at any given time and outputs a signal representative thereof to the motor controller 55, and data processor 41. Other matrix printer designs may be used in a matrix printer including a slanted print head than the one shown in FIG. 4, and also the host machine may be other than a data processor 41. The present invention is primarily concerned with the vertical-to-slant data converter 51, which will be subsequently described in much greater detail.

Again, however, there is nothing in this portion of Peer that teaches or suggests “sequentially reading one or more print data sub-elements from the memory locations associated with one pre-determined time period” and “**repeating**” the sequentially reading step “**for a subsequent pre-determined time period for each pulse generated by the pulse generating means,**” as recited in claim 1 of the present application.

Moving on, Peer at column 6, lines 5-14 states the following:

The general sequence for the program shown in flow chart form in FIG. 6 is initiated externally at the beginning of a print time. At this time, the direction in which line is to be printed, left-to-right or right-to-left, is passed to the microprocessor 77. Subsequently, the RAM 81 is zeroed,

as are the input latches 65-68, during the initialization portion of the program to prepare for receiving new columns of vertical imaging data bits from the data processor 41, in this example.

This passage of Peer merely discloses that the RAM and input latches are zeroed in order to prepare for receiving new columns of vertical imaging data bits from the data processor. Similar to the portions of Peer discussed above, however, this passage does not teach or suggest “sequentially reading one or more print data sub-elements from the memory locations associated with one pre-determined time period” and “repeating” the sequentially reading step **“for a subsequent pre-determined time period for each pulse generated by the pulse generating means,”** as recited in claim 1 of the present application.

The remaining part of the cited passage, namely Peer at column 6, lines 14-30, states the following:

After the initialization portion of the program, the print loop is entered, wherein at every vertical column throughout the line of print, new imaging data bits are externally latched and then written into the RAM 81 from the latches 65-68 as directed by an input address pointer P_i , while data in the RAM 81 is read out from the RAM memory banks 87-90 as directed by an output address pointer P_o . The output data bits are sequentially latched into the buffer output latches 93-100. Thereafter, in response to a fire signal being applied to the drive pulse generator 102 from the data processor, the latched data bits within the buffer output latches 93-100 are transferred into the final output latch 101. Also at this time, the drive pulse generated by the drive pulse generator 102 enables the final output latch stage 101 to output its data bits as control signals for operating the print element drivers 53.

While Peer discloses that the “drive pulse generated by the drive pulse generator 102 enables the final output latch stage 101 to output its data bits as control signals for

operating the print element drivers 53,” this does not equate to the limitation recited in claim 1 of the present application. That is, this portion of Peer does not teach or suggest “sequentially reading one or more print data sub-elements from the memory locations associated with one pre-determined time period” and “repeating” the sequentially reading step “**for a subsequent pre-determined time period for each pulse generated by the pulse generating means,**” as recited in claim 1 of the present application.

Next, Peer at column 8, lines 35-40 states the following:

The drive pulse generator 102 is responsive to a “fire signal” from the data processor 41 for providing the pulse timing required for operating the print element drivers 53. Typically, the drive pulse generated by pulse generator 102 is either a single or double pulse, depending upon the application.

This passage of Peer merely states that a drive pulse generator is responsive to a fire signal in order to provide a pulse timing requiring for operating the print element drivers. Similar to the passages above, however, this passage does not recite all of the limitations that the Office Action acknowledges are missing from Slomianny. That is, this passage does not reach or suggest “sequentially reading one or more print data sub-elements from the memory locations associated with one pre-determined time period” and “**repeating**” the sequentially reading step “**for a subsequent pre-determined time period for each pulse generated by the pulse generating means,**” as recited in claim 1 of the present application.

As noted above, the Office Action also cites Figure 6 of Peer as disclosing the limitations noted above. Figure 6 of Peer shows the following:

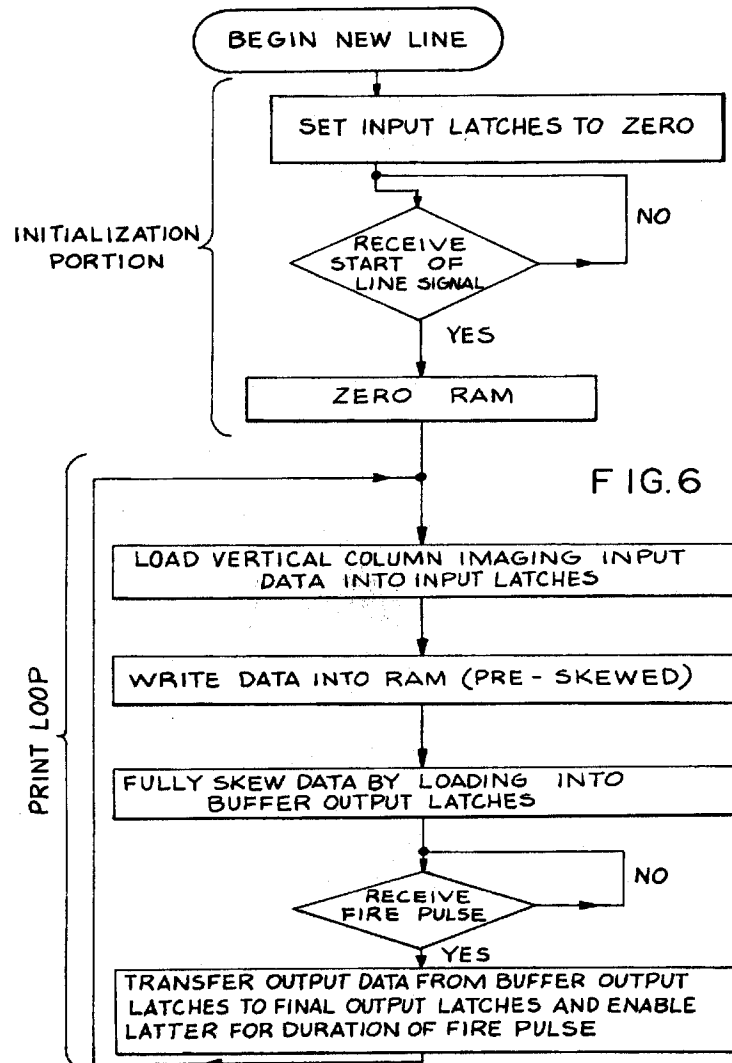


Figure 6 is a "flow chart showing the program control for one embodiment of the present invention." See Peer at column 3, lines 13-14. As shown above, however, there is nothing in Figure 6 that teaches or suggests "sequentially reading one or more print data sub-elements from the memory locations associated with one pre-determined time period" and "repeating" the sequentially reading step "for a subsequent pre-determined time period for each pulse generated by the pulse generating means," as recited in claim 1 of the present application.

In providing further explanation for the claim rejections, the Office Action states the following:

Peer discloses new imaging data bits are externally latched and then written into the RAM/memory (81) from the latches (65-68), and then the output data bits are sequentially latched into the buffer output latches (93-100) from the RAM/memory (81) banks (sequentially reading one or more print data sub-elements from the memory locations). Thereafter, in response to a fire signal applied to the drive pulse generator (pre-determined period), the latch data bits within the buffer output latches (93-100) are transferred into the final output latch and enables the final output latch stage to output its data bits as control signals for operating the print element drivers; and repeating the sequentially reading step for a subsequent pre-determined time periods (print loops) for each pulse generated (fire pulse) by the pulse generating means (Figure 6; Column 6, Line 5-30; Column 8, Lines 35-40)

February 26, 2007 Office Action at page 5. Initially, the Office Action does not explain how a “fire signal applied to the drive pulse generator” is a “pre-determined time period.” Nor does the Office Action explain how a “print loop” and a “fire pulse” represent repeating a sequentially reading step for a subsequent pre-determined time period for each pulse generated by a pulse generating means.

The Applicants respectfully submit that Peer does not teach or suggest, nor does the Office Action clearly explain how Peer discloses, “sequentially reading one or more print data sub-elements from the memory locations associated with one pre-determined time period” and “**repeating**” the sequentially reading step “**for a subsequent pre-determined time period for each pulse generated by the pulse generating means,**” as recited in claim 1 of the present application. Thus, for at least the reasons discussed above, the Applicants respectfully submit that the Office Action has not established a prima facie case of obviousness with respect to the pending claims.

For at least the reasons discussed above, the Applicants respectfully submit that the proposed combination of Slomianny and Peer does not render claim 1 and 2 unpatentable. For similar reasons, the proposed combination does not teach or suggest “(f) sequentially reading each raster signal sub-element from the memory locations associated with one pre-determined time period... characterized in that step (f) is repeated for a subsequent pre-determined time period for each pulse generated by the pulse generating means,” as recited in claim 3. Thus, the Applicants respectfully submit that the proposed combination of Slomianny and Peer does not render claims 3 and 4 unpatentable.

II. A Motivation Or Suggestion To Combine The References Has Not Been Properly Identified

Turning now to the motivation to combine the references, Federal Circuit case law and the MPEP require that the “teaching or suggestion to make the claimed combination and the reasonable expectation of success must **both be found in the prior art, and not based on applicant’s disclosure.**” See Manual of Patent Examining Procedure (MPEP) at § 2142, citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added).

“In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is **not** whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious.” MPEP at § 2141.02. The law is well settled that “obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, **absent some teaching or suggestion or incentive to do so.**” *ACS Hospital Systems, Inc. v. Montfiore Hospital*, 732

F.2d 1572, 1577, 221 USPQ 929 (Fed. Cir. 1984) (emphasis added). **It is not permissible to pick and choose among the individual elements of assorted prior art references to re-create the claimed invention**, but rather “some teaching or suggestion in the references to support their use in the particular claimed combination” is needed. *Symbol Technologies, Inc. v. Opticon, Inc.* 935 F.2d 1569, 1576, 19 USPQ2d 1241 (Fed. Cir. 1991).

The Office Action, however, fails to identify anything in the prior art that would lead one of ordinary skill in the art to combine Slomianny with Peer. Instead, the Office Action summarily concludes the following:

At the time the invention was made it would have been obvious to a person of ordinary skill in the art to incorporate the teaching of Peer into the device of Slomianny, for the purpose of driving a slanted print head of a printer with a system having a low component count via the use of a microprocessor and a short processing time via unconventional microprocessor-memory-I/O design and implementation.

See February 26, 2007 Office Action at page 4. The Office Action does not offer any citations with respect to the proposed motivation. Rather, the Office Action concludes that one would be motivated to combine certain alleged elements of the references by summarizing elements allegedly disclosed in those references.

Merely identifying isolated elements in the prior art, however, is not enough to establish a *prima facie* case of obviousness:

[M]ere identification in the prior art of each element is insufficient to defeat the patentability of the combined subject matter as a whole. [*In re Rouffet*, 149 F. 3d 1350] at 1355, 1357 [(Fed. Cir. 1998)]. Rather, to establish a *prima facie* case of obviousness based on a combination of elements disclosed in the prior art, the Board must articulate the basis on which it concludes that it would have

been obvious to make the claimed invention. *Id.* In practice, this **requires** that the Board “explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious.” *Id.* at 1357-59. This entails consideration of both the “scope and content of the prior art” and “level of ordinary skill in the pertinent art” aspects of the Graham test.

When the Board does not explain the motivation, or the suggestion or teaching, that would have led the skilled artisan at the time of the invention to the claimed combination as a whole, we infer that the Board used hindsight to conclude that the invention was obvious. *Id.* at 1358.

See in re Kahn, 441 F.3d 977 (Fed. Cir. 2006) (emphasis added).

As shown above, the Office Action merely concludes that one would be motivated to combine Peer and Slomianny merely because those references allegedly disclose certain elements (without citing any evidence within the references themselves, or the prior art in general) *See* February 26, 2007 Office Action at page 4. The Office Action does not explain, however, the motivation, suggestion, or teaching to combine these references. Instead, the Office Action bases its support for a motivation to combine the references on unsupported, convenient assumptions about a person of ordinary skill in the art. Merely reciting the claim language and/or identifying isolated elements from references is not enough to establish a *prima facie* case of obviousness. “[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements.” *See id.* (emphasis added). Thus, for at least this reason, the Applicants respectfully submit that the Office Action has not established a *prima facie* case of obviousness with respect to the pending claims.

III. Conclusion

In general, the Office Action makes various statements regarding the pending claims and the cited references that are now moot in light of the above. Thus, the Applicants will not address such statements at the present time. However, the Applicants expressly reserve the right to challenge such statements in the future should the need arise (e.g., if such statements should become relevant by appearing in an Examiner's Answer to an Appeal Brief).

The Applicants respectfully submit that the pending claims of the present application should be in condition for allowance for at least the reasons discussed above, and request reconsideration of the claim rejections. Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the telephone listed below. Please charge any necessary fees or credit any overpayment to Account No. 13-0017.

Respectfully submitted

Date: April 19, 2007

By: /Joseph M. Butscher/
Joseph M. Butscher
Reg. No. 48,326
Attorney for Applicants

McANDREWS, HELD & MALLOY, LTD.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
Telephone: (312) 775-8000
Facsimile: (312) 775-8100